HALF-BRIDGE HIGH VOLTAGE GATE DRIVER PROVIDING PROTECTION OF A TRANSISTOR

BACKGROUND OF THE INVENTION

[0001] This application claims the benefit of U.S. Provisional Application No. 60/423,496, filed October 31, 2003, entitled "Half-Bridge High Voltage Monolithic Gate Driver Providing Full Protection of Power Transistor and Diagnostic Feedback," which is incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

[0002] The field of the invention is gate drivers for metal oxide silicon field effect transistors, especially gate drivers providing full protection and diagnostic feedback.

BACKGROUND OF THE INVENTION

[0003] Metal oxide semiconductor field effect transistors (MOSFETs) have been used in power electronics applications for their ability to carry large currents and to block high off-state voltages, while having comparatively low on-state voltage drops across the transistor. Generally, there are two parasitic capacitances between the gate to source and the gate to drain that may cause switching delays if the gate driver does not support large initial currents.

[0004] Conventional MOSFET gate driver circuits are simple, self-design circuits. More complex integrated circuit gate drivers are known that are controlled directly from transistor-transistor logic, complementary metal oxides semiconductors and microprocessor logic circuits. If the integrated driver circuit does not provide floating isolation, it is necessary to include a floating power supply.

SUMMARY OF THE INVENTION

[0005] A gate driver integrated circuit for switching one or more power transistors uses an external supply voltage and an external controller. The integrated circuit comprises an output stage for each of the power transistors, an input stage and a fault control circuit integrated in the integrated circuit. In operation, the output stage is coupled to the power transistor, such that a desaturation state of the power transistor may be detected, allowing a soft shutdown sequence to be executed, gradually shutting down the power transistor. Thus, transient over-voltages are prevented. The input stage is coupled to the output stages and may be coupled to the external controller, which provides an external control input for each power transistor. The input stage is configured to control the output stage as a function of the external control inputs during normal operation.

[0006] The fault control circuit is coupled to the output stage and the input stage. The fault control circuit operates to place the input stage in a hold state during the soft shutdown sequence of one or more of the output stages, causing the input stage to ignore the external control inputs from the external controller during the soft shutdown sequence. Thus, the output stages are not switched on/off by the external controller (freeze) during the soft shutdown sequence. After soft shutdown sequences are completed by the output stages, the fault control circuit may initiate a hard shutdown. The fault control circuit may also manage fault control signals with external devices, such as the external controller and other gate driver integrated circuits, connected in a network of devices, for example. Thus, the fault control circuit may insure that desaturation protection takes priority over under-voltage protection and normal operation of the output stages.

[0007] The gate driver integrated circuit is operably designed to drive a single half-bridge in power switching applications, including a gate driving

capability and low quiescent current, which enables bootstrap supply techniques in power systems. The gate driver comprises full short circuit protection by detecting power transistor desaturation. Half-bridge voltage is managed by smoothly turning off the desaturated transistor via a dedicated soft shutdown sequence, preventing transient over-voltages and reducing electromagnetic emissions.

[0008] In one embodiment, a multi-phase system of gate drivers communicate using a dedicated local network of electronic signals to manage phase to phase short circuits. For example, a system controller may force shutdown or a read device fault state by way of a 3.3 volt compatible CMOS input/output pin. Diagnostic feedback is enabled to improve signal immunity from the direct current bus noise. For example, both the control and power ground use dedicated pins enabling the low side emitter current to be sensed, and under-voltage states are independently managed in high side and low side driving circuits. The low side driving circuit is referenced to ground, and the high side driving circuit is capable of floating to a high voltage. Thus, an independent floating power supply is not required. For example, the external controller is capable of asserting control inputs HIN, LIN, which switch the gate drivers on and off during normal operation.

[0009] One advantage of a gate driver integrated circuit according to one embodiment of the present invention is that the output stages are able to turn on quickly with high current output, while being protected dynamically. Another advantage is that a bootstrap voltage is capable of supplying the high side driver circuitry by a bootstrap diode and bootstrap capacitor. Yet another advantage is that a multiphase system of gate drivers may be comprised of one gate driver integrated circuit per phase of the multiphase system using a common, dedicated local network of fault signals to coordinate fault protection of the multiphase system, such as desaturation and under-voltage fault protection.

[0010] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

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BRIEF DESCRIPTION OF THE FIGURES

[0012] Figure 1 shows one embodiment of the present invention electrically connected in a half-bridge circuit.

[0013] Figure 2 illustrates a functional block diagram of the gate driver integrated circuit shown in Figure 1.

[0014] Figure 3 illustrates a state diagram of the embodiment shown in Figure 2.

[0015] Figure 4 shows one embodiment of the fault management circuit 40 of Figure 2.

[0016] Figure 5 illustrates one embodiment of the structure of a desaturation sensing and soft shutdown circuit of Figure 2.

[0017] Figure 6 shows one embodiment of the under-voltage circuit 60 of Figure 2.

[0018] Figure 7 shows a simplified diagram of the input and output of a Schmitt trigger circuit 70 as shown in Figure 2.

[0019] Figure 8 shows one embodiment of the output circuit driving LON, HON, SSDH and SSDL of the high side and low side circuit drivers.

[0020] Figure 9 shows the high side and low side circuit drivers for the LOP and HOP signals.

[0021] Figure 10 shows the generation of an internal signal based on feedback signals, including the desaturation voltage.

[0022] Figure 11 shows generation of an internal fault hold signal and hard and soft shutdown internal signals based on inputs FAULT/SD and SY_FLT.

[0023] Figure 12 shows the switching time waveforms of the high end low side circuit drivers.

[0024] Figure 13 shows the soft shutdown timing for the high side and low side circuit drivers.

[0025] Figure 14 shows a timing diagram for desat timing.

[0026] Figure 15 shows a timing diagram for internal dead time timing.

[0027] Figure 16 shows an alternative embodiment of a bootstrap method of supplying the high side driver circuitry.

[0028] Figure 17 illustrates the input/output timing diagram with SY_FLT and FAULT/SD as output.

[0029] Figure 18 shows the input/output logic diagram with SY_FLT and FAULT/SD as input.

[0030] Figure 19 shows another embodiment of the present invention.

[0031] Figure 20 shows a graphical representation defining nomenclature.

[0032] Figure 21 shows an equivalent circuit diagram for determining the sizing of the gate on resistance R_{Gon} for analysis of the switching time t_{sw}.

[0033] Figure 22 shows another equivalent circuit diagram for determining the sizing of the turnoff resistance R_{Goff} for use in analysis for IGBT turnoff.

[0034] Figure 23 illustrates a gate drive loop.

[0035] Figures 24a through 24c show an example of a three layer printed circuit board layout for one embodiment of the present invention.

DETAILED DESCRIPTION

[0036] One embodiment of a gate driver integrated circuit 10 for driving and protecting an insulating gate bipolar transistor 110 comprises an input control stage 70, a hold logic stage 42, a switching logic stage 73, at least one gate driver output stage 50 and a fault control circuit 40. For example, the gate driver integrated circuit 10 has circuits integrated as shown in Figure 2. The input control stage 70 is electrically connected to at least one external control input capable of connecting to an external controller. The input stage 70 has at least one control output to the hold logic circuit 42, which has at least one internal hold output and an internal connection to the fault control circuit 40 for activating a hold state (freeze), causing any changes in the signals from the input stage 70 to be ignored. The hold output is received by the switching logic stage 73, which has at least one switching output to each of the output stages 50 of the integrated circuit 10. The switching logic stage is also connected to the fault control circuit 40, receiving a shutdown control signal from the fault control circuit 40. For example, activation of the shutdown control signal by the fault control circuit 40 causes an immediate, hard shutdown of all of the output stages 50 in the integrated circuit 10.

[0037] In one embodiment, at least one output stage 50 is capable of being to an external voltage V_{BS}, V_{CC} and an external desaturation voltage sensing diode 1, 2. For example, as shown in Figure 5, each gate driver output stage 50 comprises a predriver 51 and protection circuitry 52, as shown in Figure 2. In one example, the predriver 51 is integrated with the protection circuitry 52 as shown in Figure 5. The gate driver output stage 50 has a driver sourcing output V_{HOP}, V_{LOP}, a driver sinking output V_{HON}, V_{LON}, a desaturation voltage sensing circuit 56, 57, 58, 59, 61, 63 and DSH/L and a desaturation protection output V_{SSDH}.

[0038] In one example, a logic supply voltage failure is detected by an under-voltage detection circuit 60, such as the under-voltage detection circuit shown

in Figure 6. If a supply voltage under-voltage failure is detected by the detection circuit 60, the fault control circuit 40 disables the output stages 50, providing under-voltage protection. In one embodiment, an under-voltage event of the logic supply voltage V_{CC} disables both the low side and high side output stages 50. For example, under-voltage detection generates a diagnostic signal by forcing a dual function input/output pin FAULT/SD active low. In this example, the fault state is not latched and the dual function input/output pin FAULT/SD is released when the logic supply voltage V_{CC} is no longer in an under-voltage state.

[0039] In another example, during an under-voltage state of the high side gate driver floating supply V_{BS}, a high side under-voltage protection circuit in the protection circuitry 52 disables only the high side output stage 50 latching the output stage 50 off, but allowing the low side output stage to switch the low side transistor 7 or to generate diagnostic signals. For example, the high side remains latched until external control input HIN is received from the external controller.

[0040] Desaturation protection of the gate driver integrated circuit 10 protects a power transistor, such as an insulating gate bipolar transistor 110, from transient voltages during transistor switch-off. For example, a phase and/or a rail supply short circuit induce overload states that may cause a transistor failure. For example, inducing large current increases in an insulating gate bipolar transistor, may cause the transistor to desaturate, which may be detected as an increase of the emitter to collector voltage V_{CE}. The current in a power transistor in a desaturated state may be as high as ten times the nominal current, for example. Thus, when the transistor is switched off, the high current may generate a high voltage transient in the output stage. The high current should be reduced to protect against over-voltage states. In one example, a gate driver integrated circuit protects against over voltage states by smoothly and gradually turning off the desaturated transistor using a soft shutdown sequence, using the SSD H/L connection of Figure 5, for example. An

external sensing diode 1, 2 has a voltage rating greater than the maximum supply voltage and a low stray capacitance such that noise coupling and switching delays are reduced. The sensing diode 1, 2 is biased by an internal pull up resistor 59, as shown in Figure 5. For example, the internal pull up resistor 59 should equal the quotient of the voltage V_{CC}, V_{BS} across the transistor 6, 7 and the low input bias current I_{DS}..

[0041] Figure 5 shows one structure for desaturation sensing and soft shutdown. For example, the switching control signal is received by the output stage 50 either directly from the shutdown logic circuit 73 or via a level shifter 22, as shown in Fig. 2. The desaturation signal DESAT HS/LS is provided to the fault control circuit 40, which helps to control the hold logic 42 and the shutdown logic circuit 73, as shown in Figures 2 and 4. For example, the configuration of the desaturation sensing and soft shutdown circuitry for the high and low side output stages 50 may be the same.

[0042] In one embodiment, the high and low desaturation voltages V_{DSH}, V_{DSL} are automatically clamped by being internally biased to the local supply. When the emitter to collector voltage V_{CE} increases, the voltage at the desaturation pin V_{DSH}, V_{DSL} increases also. When V_{DSH} or V_{DSL} exceeds a threshold voltage V_{DSAT}, the desaturation comparator 57 triggers, which may initiate a soft shutdown sequence. For example, the comparator output is filtered to avoid desaturation fault detection erroneously induced by external noise. In one example, noise that has a pulse length shorter than a threshold time is filtered. In another example, the desaturation circuit is disabled by a blanking signal 63, preventing any desaturation detection by transients during transistor turn-on. An example of propagation and timing delays of one embodiment is shown in Table VI.

[0043] In one embodiment, the fault control circuit 40 asserts an external hold by asserting an external desaturation fault output SY_FLT during a soft shutdown. Thus, an external dedicated local network reports the soft shutdown state

during the entire soft shutdown sequence to other devices connected to the network. After soft shutdown is complete, the external hold signal SY_FLT is released, and an external hard shutdown signal FAULT/SD may be asserted, generating a hard shutdown of all the output stages. After a hard shutdown, each output stage may be latched low until the fault is cleared, such as by raising the voltage at the fault clear connector FLTCLR.

[0044] After asserting a fault clear input FLTCLR, the external controller may reinitiate normal operational control of the gate driver integrated circuits 10, 10', 10" using the input controls HIN, LIN. For example, during normal operation the external controller asserts switching control inputs HIN, LIN such that the high side power transistors are switched on and off by the gate driver integrated circuits 10, 10', 10" in a multiphase system, as shown in Figure 19.

[0045] In one embodiment, under-voltage fault protection and external hard shutdown are masked during a soft shutdown sequence, as shown in the fault control circuit of Figure 4. Thus, desaturation protection is an independent and overriding process that is disabled only when the output status is off or during transients defined by the filters in the output stages 50, as described previously.

[0046] As shown in Figure 5, the predriver 51 may comprise two turn-on switches 53, 54 and one turn-off switch 55. A first turn-on switch 54 is constantly asserted while the second turn-on switch 53 is maintained active only for a limited time t_{ON1}. In this embodiment, the second switch boosts the total driving capability, accommodating both fast gate charging to the plateau voltage and transient voltage control during switching. A single turn-off switch 55 offers a low impedance path, which prevents self turn-on due to parasitic Miller capacitance in the power switch, for example.

[0047] In an alternative embodiment, a dedicated circuit provides an active bias as shown in Figure 10. Active biasing is used in the sensing and

desaturation circuit of the output stage 50, as shown in Figure 10. In a high side circuit, the desaturation biasing current may become relevant for dimensioning a bootstrap capacitor 12, which is shown in Figure 1. If the value of the pull up resistor R_{DSH}, R_{DSL} in a non-actively biased circuit is too low, the bootstrap capacitor 12 may be discharged significantly by a high current across the pull up resistor R_{DSH}, R_{DSL}. Thus, the resistance of the pull up resistor R_{DSH}, R_{DSL} is selected to be at least about 100 kiloOhms (kΩ). The change in voltage with time applied by the power transistor 6, 7 during commutation may inject considerable current, because the impedance is only controlled by the pull up resistor R_{DSH} when the transistor is off, resulting in considerable current injected through stray capacitance of the diode 1 into the desaturation detection pin DSH. Active biasing reduces this noise. For example, a dedicated biasing current is selected that reduces the impedance on the desaturation detection pin DSH, when the voltage exceeds the desaturation threshold voltage V_{DESAT}. In one embodiment, the impedance is reduced from about 100 kΩ to only about 100 Ohms (Ω), which helps to reject the noise caused by current injection by the parasitic capacitance. When the power transistor is fully on, the sensing diode gets forward bias and the voltage at the desaturation pin DSH decreases. At this point, the active biasing circuit deactivates, reducing the bias current through the sensing diode 1.

[0048] In another embodiment, more than one gate driver integrated circuit is used in a multi-phase system, as shown in Figure 19, for a three phase example. A bidirectional desaturation fault input/output SY_FLT is connected by a local dedicated network, such as a bus, to each gate driver integrated circuit 10. Then, if desaturation is detected and a desaturation fault output SY_FLT is asserted by one of the integrated circuits 10, then the desaturation fault state of one gate driver integrated circuit 10 is read by each of the other gate drivers integrated circuits. Thus, the other output stages 50 enter a hold state, regardless of the input

signals HIN, LIN received from the external controller. In case of a phase to phase short circuit where two insulating gate bipolar transistors are involved, this prevents a hard shutdown while one gate driver is in a soft shutdown state, which prevents a vanishing soft shutdown. However, the output stages 50 that are in a hold state are not completely inactive, because desaturation detection takes the highest priority overriding a hold state (freeze), as shown in Figures 3 and 4. Thus, the local network for the desaturation fault output SY_FLT may be a local network solely between the drivers need not be connected to the external controller.

[0049] In one embodiment, another bidirectional fault indicator FAULT/SD may be connected in a network with each of the other gate drivers and the system controller. When asserted, the shutdown fault output FAULT/SD commands a hard shutdown of all of the output stages 50 of each of the gate driver integrated circuits 10, 10', 10". For example, there are three events that can force a hard shutdown:

1. Desaturation Detection Event. The FAULT/SD connection is latched low when the soft shutdown sequence is completed, and only a fault clear input FLT_CLR from the external controller is capable of resetting the gate controllers. According to this example, the external controller must be connected to the FAULT/SD network and to the FLT_CLR connection of each gate driver 10.

2. Under-voltage on the Fixed Supply Voltage V_{CC}. The FAULT/SD connection is forced low and held low until the supply voltage returns above the under-voltage threshold (not latched). When a plurality of gate drivers 10 are connected to a FAULT/SD network, then the FAULT/SD connection may generate an external fault to other gate drivers 10.

3. External Fault. The FAULT/SD pin is externally driven low either by the controller or by another gate driver integrated circuit (not latched). When the

controller or the other gate driver 10', 10" deactivates the FAULT/SD pin, then the gate driver 10 may return to normal operating mode.

[0050] In one example, as shown in Figure 1, a gate driver integrated circuit 10 is electrically connected to a 1200 volt DC bus V_B and a 15 volt power supply is bootstrapped using a bootstrap diode 11 connected to the logic supply voltage V_{CC} connector and the high side supply voltage V_B connection and a bootstrap capacitor 12 which is connected between V_B and the high side offset voltage V_S connection. Three gate resistors 13, 14, 15 are attached to the high side pins HOP, HON and SSDH pins, respectively. Three more gate resistors 16, 17, 18 are attached to low side pins LOP, LON and SSDL, respectively.

[0051] For example, three gate resistors 16, 17, 18 are placed close together and the gate loop area 5 defined by the area between the gate resistances, the drain of a MOSFET and the voltage connected to the drain of the MOSFET is reduced, reducing electromagnetic noise. Otherwise, unnecessary electromagnetic noise may be generated by the gate drive loop 5 acting as an antenna, receiving and transmitting electromagnetic waves. Also, current may be injected inside the gate drive loop 5 via collector-to-gate parasitic capacitances of an insulating gate bipolar transistor (IGBT).

[0052] Parasitic auto-inductance of the gate loop 5 may contribute to development of a voltage across the gate emitter, which increases the possibility of self turn-on. Therefore, the grouping of the high side gate driver and the low side gate driver pins, such as shown in Figure 1, allows the gate drive loop areas 5 to be reduced, reducing the chances for undesirable self turn-on of the transistor 6, 7.

[0053] Figure 2 illustrates a block diagram of a gate driver integrated circuit 10. The control pins 9 include high side input logic pin (HIN), low side logic input pin (LIN), a dual function input/output active low pin (FAULT/SD), another dual function input/output active low pin (SY_FLT) and a fault clear active high

input (FLT_CLR). Separate logic control input pins HIN, LIN allow the high side and low side gate drivers to be controlled independently of each other by an external controller (not shown).

[0054] The FAULT/SD pin has a dual function, indicating a fault state as an output and shutting down the output of the gate drivers regardless of HIN or LIN status as an input, for example. The SY_FLT pin also has a dual function, indicating occurrence of a soft shutdown sequence as an output and activating a hold on the output status of both the high side and low side (freeze state) as an active low input signal, for example.

[0055] For example, the logic of the fault control circuit 40 is shown in Figure 4, and the timing and logic diagrams of Figures 17 and 18 show the resulting effect on the integrated circuit 10. Referring to Figure 17, an input/output timing diagram is shown with SY_FLT and FAULT/SD as output signals. When the input signals HIN and LIN are both on, the output signals are turned off, providing anti-shoot through protection, as shown at position A. At position B, the high output signal is on and the high side IGBT desaturates, e.g. DSH goes active high, causing SY_FLT output to register active low. The high output shuts down softly while the SY_FLT output signal stays low. Then, when the SY_FLT goes high, the fault control circuit 40 asserts the shutdown fault FAULT/SD low. While in soft shut-down, the low output is placed in a hold state (freeze) by the fault control circuit 40, even if the external controller asserts or deactivates input control LIN. After soft shutdown, the fault control circuit 40 latches a hard shutdown FAULT/SD. While FAULT/SD is latched low, the FLT_CLR pin may be asserted to disable the FAULT/SD, resetting the fault control circuit 40 and allowing the output to return to following the inputs, as shown after position C in the timing diagram of Figure 17. At position D, the high side DS pin input voltage (DSH) becomes high, but the high DSH is not read since the high side output voltage HOP, HON is off.

[0056] At position E, the low side output voltages LOP, LON are on, when the low side desaturation input voltage DSL becomes active high. Thus, low side IGBT desaturation is detected, and the low side output voltages LOP, LON shut down softly (gradual shut down via SSDL), while the SY_FLT output signal is asserted low by the fault control circuit 40. When SY_FLT is released, then the fault control circuit 40 asserts the shutdown fault FAULT/SD low. During the soft shutdown sequence, changes in the external control inputs HIN, LIN are ignored. After completing the soft shutdown sequence, the fault control circuit 40 asserts a hard shutdown FAULT/SD, which is later cleared FLT_CLR by the external controller.

[0057] Figure 18 shows the logic diagram with SY_FLT and FAULT/SD as inputs. At position A, the device 10 is in a hold state, regardless of input variations. The hold state is forced by externally forcing SY_FLT low. Thus, during the hold state, changes in the low and high side logic input voltages HIN, LIN are frozen by the fault control circuit 40, having no effect on the output stages 50. At position B, the device 10 has all output voltages turned off by the fault control circuit 40 in response to the assertion of an externally-driven, active-low shutdown fault signal FAULT/SD. At position C, assertion of FLT_CLR has no effect, because FLT_CLR to the local gate driver integrated circuit 10 does not disable an active, external hard shutdown state. At position D, the external FAULT/SD signal is released, and the output voltages HOP, HON, LOP, LON return to following the control input voltages HIN, LIN. Since the external hard shut-down state is not latched by the fault control circuit 40 of the local gate driver integrated circuit 10. Reasserting FAULT/SD by externally driving the FAULT/SD pin low causes another hard shut-down at point E. Externally forcing SY_FLT low at point F, once again puts the integrate circuit 10 into a hold state, freezing the status of the high and low

output voltages, until the external SY-FLT is released, and an external FAULT/SD is asserted, shutting down the output stages 50.

[0058] Figure 3 shows a logic map of the various states of one embodiment of the present invention. On the high side output stage, an under-voltage state is determined for high side voltage difference V_{BS}, which is the difference between floating supply voltage V_B and high side offset voltage V_S. On the low side output stage, an under-voltage state is detected for the low side supply voltage V_{CC}. System variables, such as FLT_CLR, HIN, LIN, low side under-voltage, UV_V_{CC}, high side under-voltage UV_V_{BS}, DSH, DSL, SY_FLT and FAULT/SD, are shown as signals labeled on the lines of Figure 3. The logic states are shown within the ovals. A change of logic value of the signal shown on the lines in Figure 3 generates a state transition. For example, when the device is presently in an under-voltage V_{BS} state 130, the signal UV-V_{BS} 131 is asserted and the high output is shut down by the output side gate driver circuit 50 of Figure 2. For example, the only way for the high side output voltages HON, HOP to turn on is if a rising edge event is asserted in the high side input voltage logic HIN.

[0059] Regarding Figure 4, DesatHS and DesatLS are internal signals originating from the high side and low side gate drivers 50. The Desat logical OR gate 91 is on if either DesatHS or DesatLS is asserted. The logical state of the OR gate 91 is input to a logic switch circuit 92, an intermediate OR gate 93 and the gate of transistor 96, which takes SY_FLT low by switching to V_{SS}. Thus, an internal hold signal is asserted and passed from the logic management circuit 40 to the hold stage 42 of the input stage 71, as shown in Figure 2. For example, during soft shutdown control logic inputs, under-voltage fault and external hard shutdown are masked until the end of soft shut-down by the logic elements 92, 93, 94, 95 and 98 of the fault control circuit 40 and the internal hold stage 42. Thus, desaturation

protection works independently of the external controller and under-voltage protection measures.

[0060] Figure 5 illustrates one embodiment of a gate driver output stage that may be used for either the high side or the low side output stages 50. The pre-driver 51 controls operation of the output switching transistors 53, 54, 55. The remainder of the circuit provides local desaturation protection and soft shutdown circuitry via external desaturation detection connection DesatHS/LS. The external sensing diode 1, 2 is biased by an internal pull-up resistor 59 or, alternatively, by an active dias circuit (e.g. Figure 10) for actively biasing the sensing diode as discussed in a previous embodiment. The IGBT collector to emitter voltage (V_{CE}) of the power transistor 110 is monitored by the sensing diode 1, 2, allowing the gate driver output stage 50 to smoothly turn off a desaturated transistor 110 using the SSD H/L pin for a soft shutdown. Thus, a desaturated transistor 110 is protected from transient over-voltage.

[0061] In the embodiment shown in Figure 5, when V_{CE} increases, the sensed voltage V_{DSH}, V_{DSL} at the desaturatation pin DSH, DSL increases also. Being internally biased to the local supply, the sensed voltage V_{DSH}, V_{DSL} at the desaturation pin DSH, DSL is automatically clamped. If the sensed voltage V_{DSH}, V_{DSL} exceeds the desaturation voltage threshold V_{DESAT} of the desaturation comparator 57, then the desaturation comparator 57 is triggered. In one embodiment, a noise filter 61 is used to avoid false desaturation detection by externally induced noise, filtering pulses shorter than the pulse width of the desaturation trigger 58.

[0062] In one embodiment, during IGBT turn-on, the desaturation circuit is disabled by a blanking signal from a blanking circuit 62 that is connected to the on/off signal for avoiding false desaturation during IGBT turn-on. The blanking circuit 62 disables the trigger 58 for a blanking period t_{BL}, which may be a predetermined maximum IGBT turn-on time, for example. Gate resistances should

be sized to avoid incomplete saturation after the predetermined blocking time $t_{BL.}$ Otherwise, desaturation detection may shutdown the output stage 50 inadvertently during IGBT turn-on.

[0063] While in a soft shut-down sequence, the output stage 40 goes into high impedance, and the pull down switch 56 is asserted to turn off the IGBT via the soft shut-down pin SSDH, SSDL. The fault control circuit asserts a desaturation fault at SY_FLT output pin (e.g. active low), externally reporting the soft shutdown status on the dedicated local network during the entire soft shutdown sequence, which continues for a shutdown period t_{SS}, for example. Then, the fault control circuit 40 releases the desaturation fault output SY_FLT and generates a shutdown fault signal FAULT/SD internally and externally. By activating the internal shutdown fault signal FAULT/SD, a hard shut-down is latched for the high and low output stages 50 by the shutdown stage 73. For example, the gate driver integrated circuit 10 is latched low until the fault is cleared, by the external controller asserting a fault clear signal FLT_CLR, which prompts the fault control circuit 40 to reset the integrated circuit 10 using logic switch circuit 92.

[0064] The high side floating supply voltage V_B provides the voltage supply to the high side driver circuitry. This supply sits on top of the offset voltage V_S. Thus, the high side floating supply voltage V_B and the offset voltage V_S provide the high side supply volage V_{BS}.

[0065] Using a bootstrap supply voltage has the advantage of being simple and low cost; however, the method is limited by the requirement to refresh the charge in the bootstrap capacitor 12. Proper bootstrap capacitor 12 selection helps to reduce limitations on the duty-cycle and on-time of the output stages, which is limited by a need to refresh the bootstrap capacitor 12.

[0066] To size the bootstrap capacitor 12, the first step is to establish the minimum voltage drop (ΔV_{BS}) that is needed when the high side IGBT is on. If

V_{GEmin} is the minimum gate emitter voltage we want to maintain, the voltage drop if found by:

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GE\min} - V_{CEon}$$

under the condition:

$$V_{GE\min} > V_{BSUV-}$$

where V_{CC} is the IC voltage supply, V_F is bootstrap diode forward voltage, V_{CEon} is emitter-collector voltage of low side IGBT and V_{BSUV-} is the high-side supply under-voltage negative going threshold.

[0067] Now, consider the factors that influence a decrease in V_{BS}:

- IGBT turn on required Gate charge (Q_G);
- IGBT gate-source leakage current (I_{LK_GE});
- Floating section leakage current (I_{lk})
- Bootstrap diode leakage current (I_{LK_DIODE});
- Desat diode bias when on (I_{DS-})
- Charge required by the internal level shifters (Q_{LS}); typical 20nC
- Bootstrap capacitor leakage current (I_{LK_CAP});
- High side on time (T_{HON}).

[0068] I_{LK_CAP} is relevant only when using an electrolytic capacitor and can be ignored if other types of capacitors are used. Preferably, at least one low ESR ceramic capacitor is used. For example, paralleling electrolytic and low ESR ceramic may result in an efficient solution.

[0069] Then, the following equation is derived:

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{QBS} + \\ + I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP} + I_{DS-}) \cdot T_{HON}$$

[0070] The minimum size of bootstrap capacitor is:

$$C_{BOOT\min} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

[0071] As one example, the following parameters are used:

a) using a 25A @ 125C IGBT (e.g. IRGP30B120KD);

- I_{QBS} = 800 μA (See Static Electrical Charact.);
- I_{lk} = 50 μA (See Static Electrical Charact.);
- Q_{LS} = 20 nC;
- Q_g = 160 nC (Datasheet IRGP30B120KD);
- I_{LK_GE} = 100 nA (Datasheet IRG30B120KD);
- I_{LK_DIODE} = 100 μA (with reverse recovery time < 100ns)
- I_{LK_CAP} = 0 (neglected for ceramic capacitor);
- I_{DS-} = 150 μA (SEE Static Electrical Charact.);
- T_{HON} = 100μs.

And:

- V_{CC} = 15 V
- V_F = 1 V
- $V_{CEonmax}$ = 3.1 V
- V_{GEmin} = 10.5 V

The maximum voltage drop ΔV_{BS} becomes

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GE\min} - V_{CEon} =$$
$$= 15V - 1V - 10.5V - 3.1V = 0.4V$$

and the bootstrap capacitor is:

$$C_{BOOT} \geq \frac{290 \text{ nC}}{0.4 \text{ V}} = 725 \text{ nF}$$

[0072] In this example, V_{CC} has been chosen to be 15V. Some IGBTs may require a logic supply voltage V_{CC} greater than 15V to work correctly with the bootstrap technique. Also, variations in V_{CC} should be considered in the above formulas, which are provided merely as an example.

[0073] The worst case for a bootstrap capacitor is when the load current I_{LOAD} is negative. Thus, the bootstrap should be sized to accommodate such a situation.

[0074] In one embodiment, a bootstrap resistor (R_{boot}) is placed in series with bootstrap diodes (see Figure 19) to limit the current when the bootstrap capacitor is initially charged. Preferably, the R_{boot} does not exceed a resistance of between 5-10 Ohms, to avoid increasing the V_{BS} time-constant t_{HON}. The minimum on time for charging the bootstrap capacitor 12 or for refreshing its charge must be verified against this time-constant t_{HON}.

[0075] For high t_{HON} designs that use an electrolytic tank capacitor, ESR must be considered. This parasitic resistance forms a voltage divider with R_{boot} generating a voltage step on V_{BS} upon charging the bootstrap capacitor 12. The voltage step and the related speed (dV_{BS}/dT) should be limited. Preferably, ESR should be designed as follows:

$$\frac{ESR}{ESR + R_{BOOT}} \cdot V_{CC} \leq 3V$$

[0076] In one embodiment, a combination of small ceramic and large electrolytic capacitors in parallel was found to acceptable, the first acting as fast charge for the gate charge only and limiting the dV_{BS}/dt by reducing the equivalent resistance while the second kept the V_{BS} voltage drop within a desired range ΔV_{BS}.

[0077] In one embodiment, a bootstrap diode had a BV> 1200v and a fast recovery time (trn < 100 ns) to reduce the amount of charge feed back from the bootstrap capacitor 12 to the fixed supply voltage V_{CC}.

[0078] The switching speed of the transistor 6, 7 can be controlled by properly sizing the resistors 13-18 controlling the turn-on and turn-off gate current. The following section provides an example for sizing the resistors to obtain a desired switching time and speed by introducing the equivalent output resistance of the gate driver (R_{DRp} and R_{DRn}).

[0079] The examples use an IGBT power transistor. Figure 20 shows the nomenclature used in the following paragraphs. In addition, V_{ge}^* indicates the plateau voltage, Q_{GC} and Q_{GE} indicate the gate to collector and gate to emitter charge, respectively.

[0080] The switching time t_{sw} is defined as the time spent to reach the end of the plateau voltage (a total $Q_{GC} + Q_{GE}$ has been provided to the IGBT gate). To obtain the desired switching time the gate resistance can be sized starting from Q_{GE} and Q_{GC}, V_{CC}, V_{GE} (see figure 21):

$$I_{avg} = \frac{Q_{GC} + Q_{GE}}{t_{sw}} \qquad \text{(I)}$$

and

$$R_{TOT} = \frac{V_{CC} - V_{ge}^*}{I_{avg}}$$

where $R_{TOT} = R_{DRp} + R_{Gon}$

R_{Gon} = gate on-resistor

R_{DRp} = driver equivalent on-resistance.

[0081] When R_{Gon} > 7 Ohm, R_{DRp} is defined by

$$R_{DRp} = \begin{cases} \frac{t_{on1}}{t_{SW}} \cdot \left[\frac{V_{CC}}{I_{01+}} + \frac{V_{CC}}{I_{02+}} \left(\frac{t_{SW}}{t_{on1}} - 1 \right) \right] & \text{when } t_{SW} > t_{on1} \\ \frac{V_{CC}}{I_{01+}} & \text{when } t_{SW} \leq t_{on1} \end{cases}$$

(I_{01+}, I_{02+} and t_{on1} from the IR2214 datasheet).

[0082] Table III reports the gate resistance size for two commonly used IGBTs (calculation made using example datasheet values and assuming V_{CC}=15V).

[0083] Turn-on gate resistance R_{Gon} may be sized to control output slope (dV_{out}/dt). While the output voltage has a non-linear behavior, the maximum output slope may be approximated by:

$$\frac{dV_{out}}{dt} = \frac{I_{avg}}{C_{RESoff}} .$$

[0084] By inserting the expression (1) and rearranging:

$$R_{TOT} = \frac{V_{CC} - V_{ge}^{*}}{C_{RESoff} \cdot \frac{dV_{out}}{dt}} .$$

[0085] As an example, table IV shows the sizing of gate resistance R_{Gon} to get dV_{out}/dt=5V/ns when using two popular IGBTs, example datasheet values and assuming V_{CC}=15V. The turn on time should be less than the blanking time t_{BL} to avoid desaturation detection during turn on.

[0086] The worst case in sizing the turn-off resistor R_{Goff} is when the collector of the IGBT in the off state is forced to commutate by external events (e.g., the turn-on of a companion IGBT). In this case the dV/dt of the output node induces a parasitic current through C_{RESoff} flowing in R_{Goff} and R_{DRn}. Figure 22 shows the current path when the low side is off and the high side turns on. If the voltage drop at the gate exceeds the threshold voltage of the IGBT, the device may self turn on, which is not desirable. Thus, the following analysis should be followed to correctly select the value of the gate turn-off resistance R_{Goff}.

[0087] The circuit of Figure 22 corresponds to the following equation:

$$V_{th} \geq \left(R_{Goff} + R_{DRn}\right) \cdot I = \left(R_{Goff} + R_{DRn}\right) \cdot C_{RESoff} \frac{dV_{out}}{dt}$$

[0088] Rearranging the equation yields:

$$R_{Goff} \leq \frac{V_{th}}{C_{RESoff} \cdot \frac{dV}{dt}} - R_{DRn}$$

[0089] When $R_{Goff} > 4$ ohm, R_{DRn} is well defined by V_{CC}/I_{O-} (I_{o-} from IR2214 datasheet). As an example, Table V reports R_{Goff} for two popular IGBT and dV_{out}/dt=5V/ns.

[0090] The examples are merely intended to provide a simple way to approximate the gate resistance sizing. A more accurate sizing may provide a more precise device model. Such models may be simulated using known circuit simulation methods.

[0091] In one example, a gate driver integrated circuit pin out maximizes the distance between floating (from DC- to DC+) and low voltage pins. Preferably,

high side components, such as resistors, diodes and IGBT are placed on the high voltage side of device, while the other components are placed on the low voltage side of the device. Also, the ground plane should not be placed near the high voltage floating side if noise coupling is to be avoided.

[0092] Current loops behave like an antenna able to receive and transmit electromagnetic (EM) noise. In order to reduce EM coupling and improve the power switch turn on/off performance, gate drive loops should be reduced. Figure 1 shows a low side gate loop 5, for example.

[0093] Moreover, current may be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop may develop a voltage across the gate-emitter increasing the possibility of self turn-on effect. Preferably, the three gate resistances are placed close together to reduce the area of the gate loop 5.

[0094] Gate driver output stages are able to quickly turn on an IGBT with up to 2A of output current, for example. In one embodiment, the supply capacitors are placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground tied supply, V_B and V_S for the floating supply) to reduce parasitic inductance/resistance.

[0095] Figure 24 shows one example of a PCB using a 3 layer PCB. Placement and routing for supply capacitors and gate resistances in the high and low voltage side reduce supply path and gate drive loops, respectively. The bootstrap diode 11 is placed under the device to have the cathode of the diode 11 as close as possible to bootstrap capacitor 12 and the anode of the diode 11 far from high voltage V_B and close to V_{CC}.

[0096] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that

the present invention be limited not by the examples herein, but only by the claims themselves.

[0097] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

TABLE I: Rated Values for an Example of a Gate Driver Integrated Circuit

Symbol	Definition	Min.	Max.	Units
V_S	High side offset voltage	V_B - 25	V_B + 0.3	V
V_B	High side floating supply voltage	-0.3	1225	
V_{HO}	High side floating output voltage (HOP, HON and SSDH)	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
COM	Power ground	V_{CC} - 25	V_{CC} + 0.3	
V_{LO}	Low side output voltage (LOP, LON and SSDL)	V_{COM} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN and FLT_CLR)	-0.3	V_{CC} + 0.3	
V_{FLT}	FAULT input/output voltage (FAULT/SD and SY_FLT)	-0.3	V_{CC} + 0.3	
V_{DSH}	High side DS input voltage	V_B -25	V_B + 0.3	
V_{DSL}	Low side DS input voltage	V_{CC} - 25	V_{CC} + 0.3	
dV_s/dt	Allowable offset voltage slew rate	-	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	-	1.5	W
Rth_{JA}	Thermal resistance, junction to ambient	-	65	°C/W
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

TABLE II: Operating Conditions for an Example of a Gate Driver Integrated Circuit

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage (Note 1)	$V_S + 11.5$	$V_S + 20$	V
V_S	High side floating supply offset voltage		1200	
V_{HO}	High side output voltage (HOP, HON and SSDH)	V_S	$V_S + 20$	
V_{LO}	Low side output voltage (LOP, LON and SSDL)	V_{COM}	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage (Note 1)	11.5	20	
COM	Power ground	-5	5	
V_{IN}	Logic input voltage (HIN, LIN and FLT_CLR)	0	V_{CC}	
V_{FLT}	Fault input/output voltage (FAULT/SD and SY_FLT)	0	V_{CC}	
V_{DSH}	High side DS pin input voltage	$V_B - 20$	V_B	
V_{DSL}	Low side DS pin input voltage	$V_{CC} - 20$	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Table III: R_{Gon} Sizing

IGBT	Q_{ge}	Q_{gc}	V_{ge*}	t_{SW}	I_{avg}	R_{tot}	R_{Gon} → std commercial value	t_{SW}
IRGP30B120K(D)	19nC	82nC	9V	400ns	0.25A	24Ω	$R_{TOT} - R_{DRp} = 12.7\ \Omega \rightarrow 10\ \Omega$	→ 420 ns
IRG4PH30K(D)	10nC	20nC	9V	200ns	0.15A	40Ω	$R_{TOT} - R_{DRp} = 32.5\ \Omega \rightarrow 33\ \Omega$	→ 202 ns

Table IV: dV_{OUT}/dt Driven R_{Gon} Sizing

IGBT	Q_{ge}	Q_{gc}	V_{ge*}	$CRES_{off}$	R_{tot}	R_{Gon} → std commercial value	$dV_{out/dt}$
IRGP30B120K(D)	19nC	82nC	9V	85pF	14Ω	$R_{TOT} - R_{DRp} = 6.5\ \Omega \rightarrow 8.2\ \Omega$	→ 4.5V/ns
IRG4PH30K(D)	10nC	20nC	9V	14pF	85Ω	$R_{TOT} - R_{DRp} = 78\ \Omega \rightarrow 82\ \Omega$	→ 5V/ ns

Table V: R_{Goff} Sizing

IGBT	V_{th} (min)	$CRES_{off}$	R_{Goff}	$dV_{out/dt}$
IRGP30B120K(D)	4	85pF	$R_{Goff} \leq 4\Omega$	→ 4.5V/ns
IRG4PH30K(D)	3	14pF	$R_{Goff} \leq 35\Omega$	→ 5V/ ns

Table VI: Example Timing Values

$V_{CC} = V_{BS} = 15V$, VS = VSS and TA = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn on propagation delay	220	440	660	ns	$V_{IN} = 0$ & 1 $V_S = 0$ to 1200V HOP shorted to HON, LOP shorted to LON, Figure 7, 10
t_{off}	Turn off propagation delay	220	440	660		
tr	Turn on rise time (C_{LOAD} = 1nF)	--	24	--		
tf	Turn off fall time (C_{LOAD} = 1nF)	--	7	--		
t_{on1}	Turn on first stage duration time	120	200	280		Figure 8
t_{DESAT1}	DSH to HO soft shutdown propagation delay at HO turn on	2000	3300	4600		$V_{HIN} = 1$ V_{DESAT} = 15V, Fig. 10
t_{DESAT2}	DSH to HO soft shutdown propagation delay after Blanking	1050	--	--		
t_{DESAT3}	DSL to LO soft shutdown propagation delay at LO turn on	2000	3300	4600		$V_{LIN} = 1$ V_{DESAT} = 15V, Fig. 10
t_{DESAT4}	DSL to LO soft shutdown propagation delay after Blanking	1050	--	--		
t_{DS}	Soft shutdown minimum pulse width of desat	1000	--	--		Figure 9

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{SS}	Soft shutdown duration period	5700	9600	13500		C_L = TBD μF, V_{DS} = 15V, Fig. 9
tSY_FLT, DESAT1	DSH to SY_FLT propagation delay at HO turn on	--	3600	--		V_{HIN} = 1 V_{DS} = 15V, Fig. 10
tSY_FLT, DESAT2	DSH to SY_FLT propagation delay after blanking	1300	--	--	ns	
tSY_FLT, DESAT3	DSL to SY_FLT propagation delay at LO turn on	--	3050	--		V_{LIN} = 1 V_{DESAT} = 15V, Fig. 10
tSY_FLT, DESAT4	DSL to SY_FLT propagation delay after blanking	1050	--	--		
t_{BL}	DS blanking time at turn on	--	3000	--		V_{HIN} = V_{LIN} =1 V_{DESAT} = 15V, Fig. 10
Dead-time/Delay Matching Characteristics						
DT	Dead-time	--	300	--		Figure 11
MDT	Dead-time matching, MDT=DTH-DTL	--	--	75		External DT=0nsec Figure 11
PDM	Propagation delay matching, Max(t_{on}, t_{off}) = Min(t_{on}, t_{off})	--	--	75		External DT> 500nsec, Fig. 7